REMARKS

In the present Application, Claims 1-8 and 12-16 are pending. Claims 1-8 and 12-16 are rejected. By this response, claims 1 and 12 are amended. In view of the following discussion, the Applicant submits that none of the claims now pending in the application are indefinite under the provisions of 35 U.S.C. §112 or anticipated under the provisions of 35 U.S.C. §102. Thus, the Applicant believes that all of these claims are now in condition for allowance.

I. Objections

The drawings are objected to as failing to show every feature of the invention specified in the claims. In particular, the Examiner states that the interposer that couples a first micro-bump in a first position in the array of micro-bumps to a first landing pad located opposite to the first position and to a second landing pad is not shown in the drawings. The Examiner also stated that a means for so coupling is not shown in the drawings. (Office Action, p. 2).

First, the Applicant has amended claims 1 and 12 to clarify that the interposer or means for coupling electrically couples the first micro-bump to the first and second landing pads. Second, the features of the interposer in Claim 1, and means for electrically coupling in Claim 12, are shown in FIG. 24. FIG. 24 shows a micro-bump ("first micro-bump" in a "first position") coupled between a signal line 1109 in the IC die 1083 and a via 1107 in an interposer 1082. The first micro-bump is electrically coupled to a landing pad ("first landing pad") on the IC package 1084 located opposite the first micro-bump through a landing pad 1103, a via 1107, a landing pad 1104, and a micro-bump coupled to the landing pad 1104. The first micro-bump is also coupled to a pad ("second landing pad") on the IC package 1084 adjacent to the first pad through the via 1107, the layer 1106, a landing pad, and the micro-bump 1105. To further clarify, the Applicant relates FIG. 24 parenthetically to the claim language at issue below:

> an interposing structure (1082) disposed inside the integrated circuit package (1084) between the integrated circuit die (1083) and the inside surface (1088) of the integrated circuit package, the interposer electrically coupling a first micro-bump (micro-bump coupled to the pad 1103) in a first position in the array of micro-bumps to a first landing pad (landing pad coupled to the landing pad 1104 through a micro-bump) located opposite to the first position and to a second landing pad (pad coupled to the micro-bump 1105) in the array of landing pads.

In view of the foregoing, the Applicant contends that the drawings show all of the features of the claimed invention. The Applicant respectfully requests that the present objection be withdrawn.

II. Rejection of Claims under 35 U.S.C. §112

Claims 1-8 and 12-16 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The Examiner states that in claims 1 and 12, it is unclear what is meant by "the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad located opposite to the first position and to a second landing pad in the array of landing pads." The Examiner requests that the Applicant explain the claimed structure as it relates to the drawings and specification. (Office Action, p. 3).

First, as noted above, the Applicant has amended claims 1 and 12 to clarify that the interposer and the means for coupling electrically couple the first micro-bump to the first and second pads. See Applicant's specification, para. [0133]. Second, the Applicant refers the Examiner to paragraph [0132] of the specification and to FIG. 24 of the drawings. Paragraph [0132] states:

> In addition to illustrating a via caposer having a bypass capacitor, Figure 24 illustrates a via caposer that redistributes signals. Figure 24 shows a fifth landing pad 1103 on first surface 1086 of caposer 1082, a fifth micro-bump 1105 on a pad on second surface 1087 of caposer 1082, and a third conductive layer 1106 within caposer 1082. Fifth landing pad 1103 is coupled to third conductive layer 1106 by a via 1107. Via 1107 is also coupled to a pad 1104 on second surface 1087. A via 1108 couples third conductive layer 1106 to fifth micro-bump 1105 through the pad on second surface 1087. Third conductive

layer 1106 comprises a conductive trace that provides a portion of a conductive path between fifth landing pad 1103 and fifth micro-bump 1105.

Although this description refers to a micro-bump on the package being coupled to landing pads opposite the IC die, the description and the claim language are electrically equivalent. That is, the vias 1108 and 1107 in FIG. 24 are electrically coupled by the layer 1106. Thus, the four micro-bumps coupled to the vias 1108 and 1007, as well as all corresponding landing pads, are electrically coupled. In particular, the micro-bump coupled to landing pad 1103 ("first micro-bump") is coupled to the landing pad on the IC package 1084 ("first landing pad") located opposite thereto, as well as a landing pad coupled to the micro-bump 1105 ("second landing pad"). In other words, the interposer is re-distributing the signal provided by line 1109 in the IC die among first and second landing pads on the IC package 1084.

In view of the foregoing, the Applicant contends that the cited language in claims 1 and 12 is clear and definite to one skilled in the art when interpreted in light of Applicant's specification. The Applicant respectfully requests that the present rejection be withdrawn.

III. Rejection of Claims under 35 U.S.C. §102

Claims 1-8 and 12-16 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,680,218 B2 to Chung et al. The Examiner separately rejected claims 1-8 and 12-15 as being anticipated by U.S. Patent No. 5,177,594 to Chance et al. These rejections are respectfully traversed.

A. Rejection under Chung

The Examiner states that Chung shows an integrated circuit package 306 having an array of landing pads on the top surface and an array of solder balls 142 disposed on the outside surface. (Office Action, pp. 4-5) (citing Chung, FIG. 5). The Examiner further states that Chung teaches an interposing structure 304 coupling a first micro-bump on a die to a first landing pad on the integrated circuit package located opposite the first micro-bump and to a second landing pad on the integrated

circuit package. (Office Action, p. 5) (citing Chung, FIG. 5). Applicant respectfully disagrees.

Chung describes an IC 302 and an IC package consisting of a vertical package section 304 and a horizontal package section 306. The IC 302 is flip-chip mounted to the vertical section 304 using solder bumps. (Chung, col. 3, line 55 through col. 4, line 18; FIG. 3). Bond pads on the bottom surface of the vertical section 304 are electrically connected to bond pads on the top surface of the horizontal section 306. (Chung, col. 5, lines 45-55; col. 8, lines 5-10). As shown in each of the Figures in Chung, the vertical section 304 couples the solder bumps of the IC 302 to the bond pads on the horizontal section 306 in a 1-1 fashion, i.e., each solder bump on the IC is coupled to one bond pad located opposite the solder bump.

In view of the forgoing, Chung does not teach or suggest each and every element of Applicant's claim 1. Namely, Chung does not teach or suggest an interposer that electrically couples a first micro-bump on the IC die to both a first landing pad located opposite the first micro-bump and to a second landing pad, each of which being on an inside surface of an integrated circuit package. In contrast, Chung describes and shows that each of the solder bumps on the IC 302 is coupled to a single one of the bond pads on the horizontal section 306. There is no teaching or suggestion in Chung that one of the solder bumps on the IC 302 is coupled to both a bond pad opposite the solder bump and another bond pad on the horizontal section.

The Examiner avers that Applicant's claim 1 does not recite that the first landing pad and the second landing pad are on the inside surface of the integrated circuit package. (Office Action, p. 9). Applicant refers the Examiner to the following language in Claim 1: "an integrated circuit package having an array of landing pads disposed on an inside surface of the integrated circuit package...." Since the first landing pad and the second landing pad are "in the array of landing pads," then the first and second landing pads are on the inside surface of the integrated circuit package.

The Examiner also specifically referred to element 516 in Chung as coupling two bond pads. (Office Action, p. 9). The bond pads referred to by the Examiner, however, are not both on the inside surface of the integrated circuit package. In Applicant's claim 1, both the first and second landing pads are part of the array of landing pads on the inside surface of the integrated circuit package.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Chung does not teach an interposer that electrically couples a first micro-bump on the IC die to both a first landing pad located opposite the first micro-bump and to a second landing pad, each of which being on an inside surface of an integrated circuit package. As such, Chung does not teach each and every element of Applicant's claim 1 as arranged therein. Accordingly, Chung does not anticipate Applicant's invention recited in claim 1.

Claim 12 includes features similar to those of claim 1 emphasized above. For the same reasons set forth above, the Applicant contends that Chung does not anticipate the invention of claim 12. Claims 2-8 and 14-16 depend, either directly or indirectly, from claims 1 and 12 and recite additional features therefor. Since Chung does not anticipate Applicant's invention as recited in claims 1 and 12, dependent claims 2-8 and 14-16 are also not anticipated and are allowable.

Therefore, the Applicant contends that claims 1-8 and 12-16 are not anticipated by Chung and, as such, fully satisfy the requirements of 35 U.S.C. §102. The Applicant respectfully requests that the present rejection be withdrawn.

B. Rejection under Chance

The Examiner states that Chance shows an integrated circuit package 54 having an array of landing pads on the top surface and an array of pins disposed on the outside surface. (Office Action, p. 7) (citing Chance, FIG. 1). The Examiner further states that Chance teaches an interposing structure 50 coupling a first micro-

bump on a die to a first landing pad on the integrated circuit package located opposite the first micro-bump and to a second landing pad on the integrated circuit package. (Office Action, p. 7) (citing Chance, FIG. 1). The Examiner states that the coupling of the first micro-bump to the second landing pad is inherent. Applicant respectfully disagrees.

Chance describes an interposer module 50 supporting an IC 52 and mounted on a ceramic interconnection substrate 54. The IC 52 and the interposer module 50 are joined to their respective surfaces by solder balls 56. (Chance, col. 4, lines 10-22; FIG. 1). Vias 64 in the interposer module 50 couple specific ones of the upper and lower solder balls 56. (Chance, col. 4, lines 40-42; FIG. 1). As shown in FIG. 1, the vias 64 in the interposer module 50 couple the solder balls of the IC 52 to the solder balls on the substrate 54 in a 1-1 fashion, i.e., each solder ball on the IC 52 is coupled to an oppositely located solder ball on the substrate 54.

In view of the forgoing, Chance does not teach or suggest each and every element of Applicant's Claim 1. Namely, Chance does not teach or suggest an interposer that electrically couples a first micro-bump on the IC die to both a first landing pad located opposite the first micro-bump and to a second landing pad, each of which being on an inside surface of an integrated circuit package. In contrast, Chance describes and shows that each of the solder balls on the IC 52 is coupled to a single one of the solder balls on the substrate 54. There is no teaching or suggestion in Chance that one of the solder balls on the IC 52 is coupled to both an oppositely located solder ball (or bond pad) and another solder ball (or bond pad) on the substrate.

The Examiner alleged that Applicant's Claim 1 does not recite that the first landing pad and the second landing pad are on the inside surface of the integrated circuit package. (Office Action, p. 9). As noted above, Applicants refer the Examiner to the following language in Claim 1: "an integrated circuit package having an array of landing pads disposed on an inside surface of the integrated circuit package...." Since the first landing pad and the second landing pad are "in the array of landing pads,"

then the first and second landing pads are on the inside surface of the integrated circuit package.

Furthermore, to establish anticipation by inherency, extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 1268 (Fed. Cir. 1991). The Examiner has not provided any evidence that Chance inherently teaches an interposer that couples a solder ball to both an oppositely located solder ball (or bond pad) and another solder ball (or bond pad) on the substrate. Notably, it is not necessarily the case, since the drawings in Chance show the exact opposite. That is, the drawings show 1-1 connectivity between the solder balls on the IC and the solder balls on the substrate.

Chance does not teach an interposer that electrically couples a first micro-bump on the IC die to both a first landing pad located opposite the first micro-bump and to a second landing pad, each of which being on an inside surface of an integrated circuit package. As such, Chance does not teach each and every element of Applicant's claim 1 as arranged therein. Accordingly, Chance does not anticipate Applicant's invention recited in claim 1.

Claim 12 includes features similar to those of claim 1 emphasized above. For the same reasons set forth above, the Applicant contends that Chance does not anticipate the invention of claim 12. Claims 2-8 and 14-15 depend, either directly or indirectly, from claims 1 and 12 and recite additional features therefor. Since Chance does not anticipate Applicant's invention as recited in claims 1 and 12, dependent claims 2-8 and 14-15 are also not anticipated and are allowable.

Therefore, the Applicant contends that Claims 1-8 and 12-15 are not anticipated by Chance and, as such, fully satisfy the requirements of 35 U.S.C. §102. The Applicant respectfully requests that the present rejection be withdrawn.

IV. CONCLUSION

Claims 1 and 12 have been amended herein. Claims 9-11 are previously cancelled. Applicant submits that none of the claims presently in the application are indefinite under the provisions of 35 U.S.C. §112 or anticipated under the provisions of 35 U.S.C. §102. Consequently, Applicant believes that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Applicant's Attorney at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent and Trademark Office on June 3, 2008.

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